

HLS Saturation Enhancement 1.0 IP Core User Guide

Revised June 20, 2018; Author Ciprian Hegbeli

1 Introduction

This user guide describes the Diligent Saturation Enhancement Intellectual Property. This IP interfaces to both the Axi-Lite and Axi-Stream in order to process a video stream and control the resolution and the saturation factor.

2 Features

- Axi- Stream 24-bit video input and output
- Axi-Lite interface for saturation and resolution control
- Resolution supported: up to 1920x1080/60Hz (clock: 148.5 MHz)
- Saturation adjustment: -0.2, 0.2, 0.4, 0.6, 0.8, 1.0, 1.2

3 Performance

The IP has been written in HLS with a target clock frequency of 150 MHz (6.67 ns) for a maximum resolution of 1920x1080. The maximum latency is at 2111405 ns with an initiation interval of 2111402 ns which is approximately one frame. The latency and initiation interval are scaled with the input resolution, meaning that a lower resolution the latency will also be lower.

4 Usage

The IP has been initially designed for a xc7z020clg400-1 target device, the resource usage for this FPGA are illustrated in

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Axi-Lite Axi-Stream
Provided with core	
Design files	C++
Simulation model	HLS Simulation
Constraints file	XDC
Software driver	Automatically generated
Tested design flows	
Design entry	Vivado™ Design Suite 2017.4
Synthesis	Vivado Synthesis 2017.4

Name	BRAM-18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	8
FIFO	0	-	115	532
Instance	7	8	7850	6809
Memory	-	-	-	-
Multiplexer	-	-	-	-
Register	-	-	-	-
Total	7	8	7965	7349
Utilization(%)	2	3	7	13

Table 1 FPGA usage

5 Overview

The IP core has been written entirely in Vivado HLS by using the HLS Video Library provided by Xilinx and a custom saturation enhancement function written by the author. In order to minimize the resource cost of the IP core, the value of the saturation have been precompiled and stored in to lookup tables. The selection of the desired saturation is done using a simple case structure which multiplexes the LUTs which will be implemented.

5.1 Processing

The input format for the image/video stream is the Axi-stream interface which can accept 24 bits of RGB data (8 bit/color) respecting the Xilinx video format. Before the actual saturation enhancement, the input stream is converted in to a matrix format with de height and width corresponding to the resolution of the input image, this is done using the HLS Video Library function *AXIvideo2cvMat*. The obtained matrix is the RGB color space, to be able to change the saturation value without effecting the other components of the image a different color space hade to be chosen; based on the functions of the HLS Video Library the HLS (hue, light saturation, aka HSL) color space has been chosen. Conversion from RGB to HLS is done using the *CvtColor* provided by the video library.

Once the saturation processing has been finished the image must be converted back to RGB color space and outputted to the Axi-Stream interface. The output Axi-Stream interface has the same format as the input Axi-Stream interface.

5.2 Saturation Enhancement

The simplest way to enhance the saturation is to multiply it by a factor, unfortunately this leads to false colors and over saturation which should be avoided if the goal is to improve a undersaturated image.

In order to avoid this a couple of additional factor have been added to the equation for saturation enhancement.

The first thing that we must take in to account is that the saturation may not overflow, therefore the maximum variable interval for a saturation component must respect the following equation:

$$var_{interval} = (MaxSaturation - src.sat)$$

Equation 1 Max interval for each pixel

The second thing which must be taken in to account is that pixels with low saturation should not be over saturated. To avoid this another variable has been added to the above equation which ensures that undersaturated value will be proportionally saturated.

$$gray_{factor} = \frac{src.sat}{255}$$

Equation 2 Gray factor condition

When choosing to desaturate the input image these additional variables don't have to be taken in to account, resulting in the following overall formula for the saturation enhancement.

$$dts.sat = \begin{cases} src.sat + fact * var_{interval} * gray_{interval}, & fact \geq 0 \\ src.sat + fact * src.sat, & fact < 0 \end{cases}$$

Equation 3 Saturation enhancement equation

Like previously mentioned the IP contain predefined LUT's for some *fact* variable which have been calculated using this function which has been implemented in to the Test Bench of the HLS project. For a visual representation of the function with the chosen fact values of the LUTs please refer to the following chart

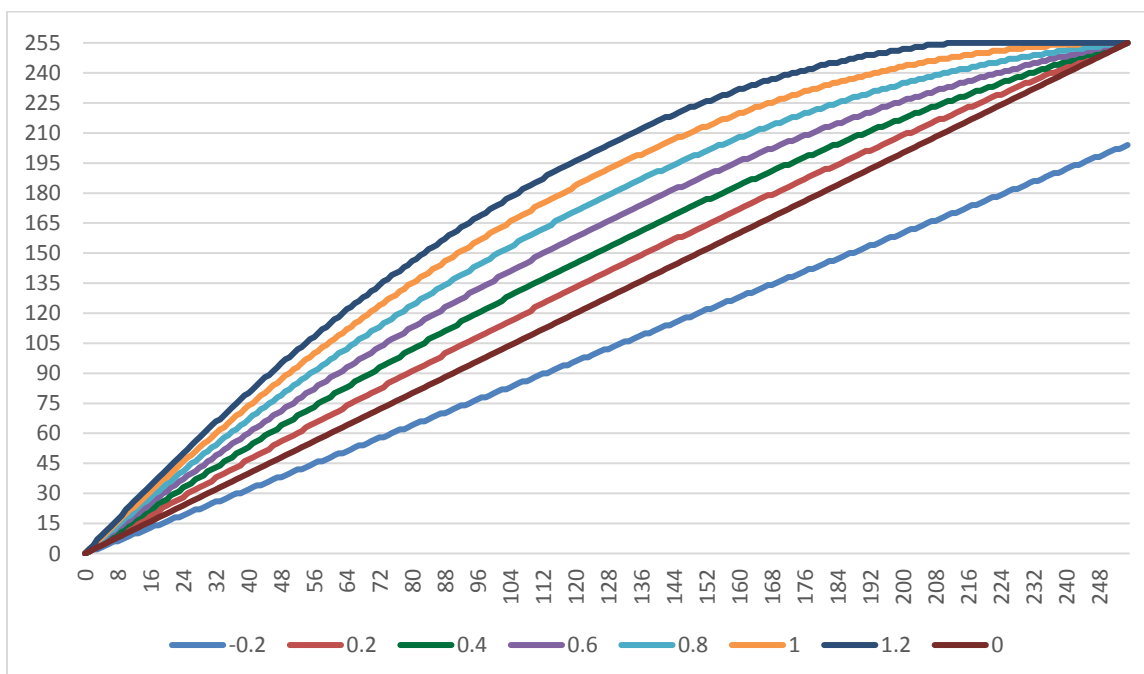


Figure 1 In/Out characteristic of saturation enhancement

5.3 HLS directives

The used directives for this IP core have been added to the source files, for further information on how they work and how to use them please refer to UG902: High-Level Synthesis by Xilinx.

5.4 Axi-Lite

The Axi-Lite interface is defined using HLS and controls three input variables of the main Saturation enhancement function. Using this interface, the user can change the resolution of both the input and the output image to a maximum of 1920x1080 and the desired saturation factor. Access to these parameters is provided via the automatically generated software driver, which respects the format of software drivers provided by Xilinx.

To change the saturation factor, the function `XHls_saturation_enhance_Set_sat` must be called. Saturation will change respecting the following rule:

Sat	Factor
0	0
1	-0.2
2	0.2
3	0.4
4	0.6
5	0.8
6	1.0
7	1.2

Table 2 Saturation selection

6 Port Descriptions

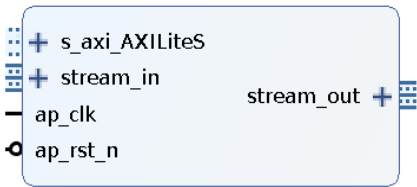


Figure 2 HLS Saturation Enhancement IP core

Signal Name	Interface	Signal Type	Init State	Description
Ap_rst_n	-	I	N/A	Asynchronous reset for the core
ap_clk	-	I	N/A	Clock for the IP core, used for Stream in/output and Axi-Lite
s_axi_AXILiteS*	Axi-Lite	I	N/A	Axi-Lite interface used to configure height, width and saturation
stream_in	Axi-Stream	I	N/A	Input video stream on 24 bits, using Xilinx video format
stream_out	Axi-Stream	O	N/A	Output video stream on 24 bits, using Xilinx video format

Table 3. Port descriptions.

7 Designing with the core

7.1 Customization

The currently IP core has been packaged for a maximum frequency of 150 MHz and a maximum resolution of 1920x1080 designed for a Zynq xc7z020clg400-1 device. For customization and further changes please create a HLS project and import all the files provided in the hls_src folder of the IP.

8 References

The following document provides additional information on the subjects discussed:

1. Xilinx Inc., UG902: High-Level Synthesis, v2017.4, February 2, 2018.