

# Zmod ADC 1410 Low Level Controller IP Core User Guide

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## 1 Introduction

This user guide describes the Diligent **Zmod ADC 1410 Low Level Controller** Intellectual Property. This IP interfaces directly with the Zmod ADC 1410 configuring the gain and coupling select relays, writing an initial configuration to the AD9648 analog to digital converter (ADC) featured by this module, demultiplexing the data received over the ADC's parallel interface and forwarding it to the user logic. The Zmod ADC 1410 Low Level Controller is intended to be used as a stand-alone IP (the stand alone mode) in projects that do not require processor interaction or it can be used in conjunction with the Diligent **Zmod ADC1410 AXI Adapter IP** that provides connectivity with the processing system.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Custom
Provided with core	
Design files	VHDL
Simulation model	N/A
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2019.1
Synthesis	Vivado Synthesis 2019.1

## 2 Features

- Initializes the hardware on the Zmod ADC 1410.
- Demultiplexes the double data rate (DDR) parallel interface featured by the Zmod ADC 1410 and exports two single data rate (SDR) channels to the user logic in the user clock domain.
- Provides the possibility of overwriting the initial ADC configuration by providing an optional upper level interface that allows indirect access to the ADC's SPI interface.
- Performs offset and gain calibration based on coefficients specified by the user/upper level IPs.

## 3 Performance

The IP is designed to forward a 400MHz clock to the ADC's clock input and expects to receive data from the ADC on a 14bit double data rate (DDR) parallel bus running at 200MSPS. Both the Zmod's ADC Channel1 and Channel2 data are multiplexed on this interface. The **Zmod ADC1410 Low Level Controller** further exports to the user logic two distinct 100MSPS single data rate (SDR) 14bit channels synchronized with the user clock domain. The Zmod ADC 1410 synchronization input (SYNC) signal is also generated by Zmod ADC1410 Low Level Controller in the AdcInClk clock domain (400MHz) allowing the ADC's sampling instant can be configured with a resolution of 2.5ns.

## 4 Overview

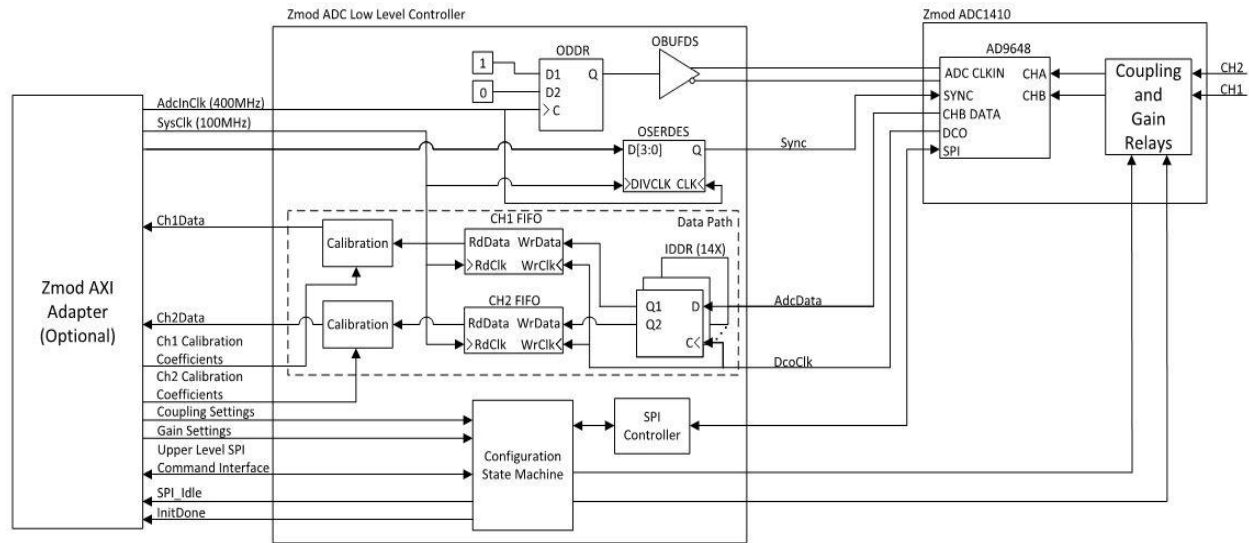


Figure 1. Zmod ADC 1410 Low Level Controller block diagram.

The structure of the IP is presented in Figure 1. The main functionalities are divided as ADC input clock generation, SYNC generation, data capture and calibration (data path) and Zmod ADC 1410 configuration (two items related with configuration functionalities will be detailed separately: the configuration state machine and the SPI controller).

### 4.1 ADC Input Clock Generation

The AD9648 on the Zmod ADC 1410 requires a differential sample clock as input. The IP is designed to forward a 400MHz which will be further divided by 4 by the ADC (option programmed in the ADC ... register by the configuration state machine). The IP does not generate the clock internally, instead it requires it as an input expecting it to be generated in the top-level design. The IP only instantiates the IO primitives required to generate the differential clock derived from it.

### 4.2 SYNC Generation

The SYNC signal allows multiple AD9648 devices to have their sample clock synchronized by resetting their internal clock dividers. An OSERDES primitive with a ratio between the divided input clock (100MHz) and the high-speed clock (400MHz) of 4 is used by the IP core to generate the SYNC signal. The ExternalSyncEn parameter enables the user to control the SYNC signal through the optional ExtSync port which represents the 4bit wide parallel input of the OSERDES primitive. The valid values that this input signal can take are "0001", "0010", "0100", "1000". If the ExtSync port is disabled, the default value of the OSERDES input will be "0001". Since the ADC clock divider is programmed by the configuration state machine to divide the input clock by 4, the ADC sampling instant can be configured with a resolution of 2.5ns. This feature can also be used for oversampling purposes.

### 4.3 Data Path

The data path consists of three stages. First, each bit of the input parallel data bus is passed to an IDDR primitive used to demultiplex the DDR interleaved format exported by the ADC (Figure 2), obtaining two SDR data channels.

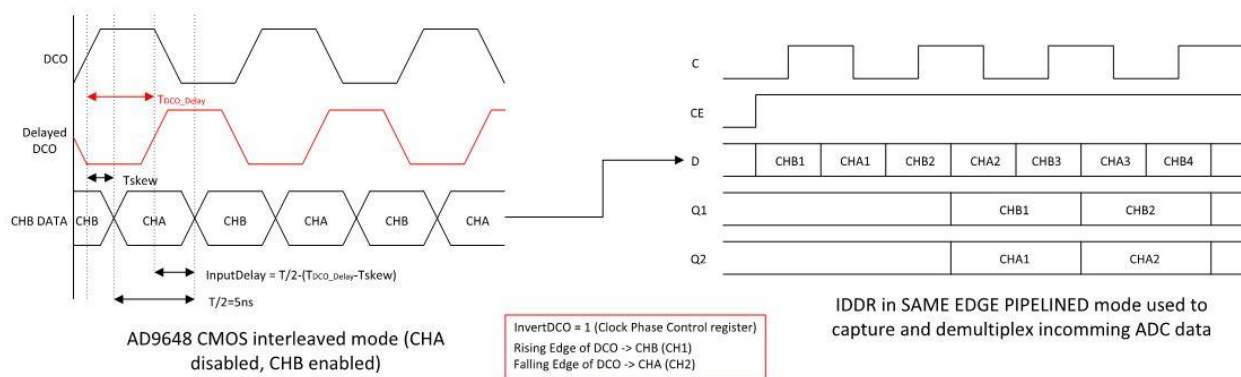


Figure 2. Input data channel demultiplexing

Each channel is further connected to a shallow FIFO used only to synchronize the received data with the IP core's system clock. The final stage is represented by the calibration stage which is responsible for compensating the offset and gain errors associated with each channel and with each gain option. The output of each channel is computed based on relation (1):

$$ChxOut = Chx_{FIFO} * CoefxMult_{LH/HG} + CoefxAdd_{LG/HG} \quad (1)$$

In the previous relation, the IP core's data output channels are labeled  $ChxOut$ , the synchronization stage outputs are labeled  $Chx_{FIFO}$  while  $CoefxMult_{LH/HG}$  and  $CoefxAdd_{LG/HG}$  represent the gain and offset calibration coefficients. The multiplicative and additive coefficients are passed by the upper layer IP Core if the **Zmod ADC 1410 Low Level controller** is used in a processor system (the external calibration interface is enabled) or they can be passed as IP core parameters otherwise. The user can obtain the calibration coefficients by booting the Eclipse board with the Linux image provided at <https://github.com/Digilent/Eclipse-Z7/releases> and run the "decutil enum" command in the command line. The Zmod ADC 1410 has to be plugged in one of the Eclipse's board SYZYGY ports.

### 4.4 AC DC Coupling and Gain Select Relay Control

The IP core provides the choice of selecting the Zmod ADC 1410 coupling and gain options statically or dynamically. For static configuration, the ExtRelayConfigEn needs to be set as "false" and the relay configuration parameters (See Table 2) need to be configured in the IP core GUI. For dynamic relay control, the ExtRelayConfigEn needs to be set as "true" and the configuration state machine will constantly monitor the external relay configuration ports and will reconfigure the AC DC coupling relays or the gain relays in response to user request.

## 4.5 Configuration State Machine

The configuration state machine first configures the AC DC coupling and gain select relays according to the values specified in the relay configuration parameters or on the external relay configuration ports as explained in Section 4.4. The next step is to send a predefined list of SPI commands to the Zmod's ADC, performing the ADC initialization. Once the initialization is complete, the state machine enters the idle state where it monitors if there is any valid data on the upper level SPI command interface or any changes on the external relay configuration ports. After reconfiguring the relays or after executing the requested SPI transfers the state machine passes the received SPI data (for read commands) and returns to the idle state. The initial configuration command sequence is listed below. After configuring each register, the register data is read back and checked against the expected value in order to determine any SPI transaction error.

1. **SPI Port config register:** Soft Reset (Address: 00h; Data: 3C)
2. **Chip ID Register:** Check ID (Read, Address: 01h; Data: -)
3. **Device Index Register:** Select CHA & CHB (Address: 05h; Data: 03h)
4. **Power modes Register:** digital reset (Address: 08h; Data: 03h)
5. **Device Index Register:** Select CHA (Address: 05h; Data: 01h)
6. **Output mode register:** Output port logic type -> CMOS 1.8V, Output interleave enable, disable port (port A), Output invert disable, Gray code (Address: 14h; Data: 32h)
7. **Device Index Register:** Select CHB (Address: 05h; Data: 02h)
8. **Output mode register:** Output port logic type -> CMOS 1.8V, Output interleave enable, Enable port (port B), Output invert disable, Gray code (Address: 14h; Data: 22h)
9. **Device Index Register:** Select None (Address: 05h; Data: 00h)
10. **Clock Divide register:** Divide by 4 (Address: 0Bh; Data: 03h)
11. **Clock Phase Control register:** Invert DCO (Address: 16h; Data: 80h)
12. **Overrange Control register:** disable overage output (Address: 2Ah; Data: 00h)
13. **Output Adjust register:** DCO and DATA 2X drive strength (Address: 15h; Data: 00h)
14. **Output delay register:** 0.56ns delay added to DCO (Address: 17h; Data: 80h);
15. **Sync control register:** SYNC enable, continuous SYNC (Address: 3Ah; Data: 02h)
16. **Device Index Register:** Select CHA & CHB (Address: 05h; Data: 03h)
17. **Power modes:** Normal operation (Address: 08h; Data: 00h)
18. **Device Index Register:** Select None (Address: 05h; Data: 00h)

## 4.6 SPI Controller

The SPI controller is designed to carry out basic register access over the AD9648's SPI interface. Only single byte data transfers are currently supported. More details about the AD9648's SPI interface can be found in [3]. The SPI controller's ports are described below.

Table 1. SPI controller port description

Signal Name	Interface	Signal Type	Init State	Description
SysClk	-	I	N/A	100MHz input clock signal.
sRst_n	-	I	N/A	Synchronous reset of negative polarity.

sSPI_Clk	SPI	O	N/A	Output SPI clock [3] divided from SysClk. Should be connected to the corresponding top-level SPI port.
sSDIO	SPI	IO	N/A	SPI SDIO signal [3]. Should be connected to the corresponding top-level SPI port.
sCS	SPI	I	N/A	SPI CS signal [3]. Should be connected to the corresponding top-level SPI port.
sRdData[7:0]	-	O	N/A	SPI register read received data
sWrData	-	I	N/A	SPI register write data.
sAddr[11:0]	-	I	N/A	SPI instruction phase address.
sWidth[1:0]	-	I	N/A	SPI instruction phase word length. The only value currently supported is 0 (1 data byte transferred).
sRdEn	-	I	N/A	Triggers a register read operation over SPI.
sWrEn	-	I	N/A	Triggers a register write operation over SPI.
sDone	-	O	N/A	Indicates that the operation requested has completed

## 4.7 Clocking

The IP is divided in three clock domains:

1. The system clock domain (100MHz), which clocks the configuration state machine, the data FIFOs read ports, the calibration logic and the Zmod ADC 1410 SPI interface.
2. The ADC input clock domain (400MHz), which is used to clock the primitives responsible with generating the SYNC signal and with passing the ADC\_InClk input clock to the Zmod ADC 1410.
3. The DCO clock domain, which is used to clock the IDDR primitives that demultiplex the ADC incoming DDR data bus and the write pots of the data FIFOs.

The IP does not constrain the clocks it requires as inputs, therefore clocks need to be constrained in the top-level design either manually or by relying on the auto-derived constraints, if using clock modifying blocks. For more information see [4].

## 5 Port description

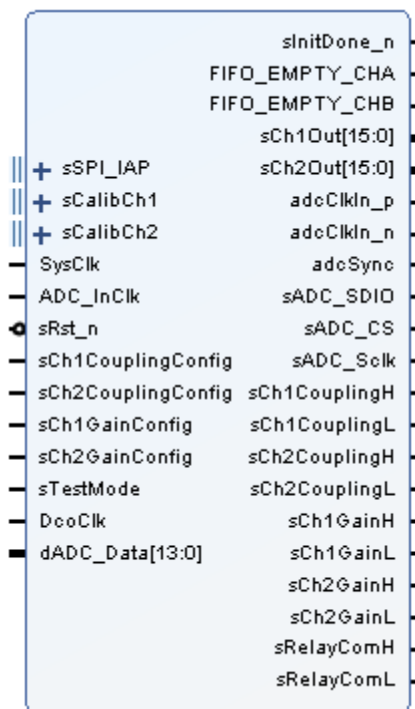


Figure 3: Zmod ADC 1410 Low Level Controller IP

Table 2. IP core port description

Signal Name	Interface	Signal Type	Init State	Description
SysClk	-	I	N/A	100MHz input clock signal.
ADC_InClk	-	I	N/A	400MHz input clock signal.
sRst_n	-	I	N/A	Synchronous reset of negative polarity.
sInitDone_n	-	O	N/A	Active low flag indicating when the Zmod initialization is complete.
sCh1Out[15:0]	-	O	N/A	16bit output data for Zmod Channel1; synchronous with SysClk.
sCh2Out[15:0]	-	O	N/A	16bit output data for Zmod Channel2; synchronous with SysClk.
sExtCh1LgMultCoef	-	O	N/A	Channel1 low gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh1LgAddCoef	-	O	N/A	Channel1 low gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh1HgMultCoef	-	O	N/A	Channel1 high gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".

sExtCh1HgAddCoef	-	O	N/A	Channel1 high gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2LgMultCoef	-	O	N/A	Channel2 low gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2LgAddCoef	-	O	N/A	Channel2 low gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2HgMultCoef	-	O	N/A	Channel2 high gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2HgAddCoef	-	O	N/A	Channel2 high gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sCh1CouplingConfig	-	O	N/A	Channel1 AC DC coupling select external port. This port is enabled by setting the ExtRelayConfigEn parameter to "true". <ul style="list-style-type: none"> <li>• 1 = AC coupling.</li> <li>• 0 = DC coupling.</li> </ul>
sCh2CouplingConfig	-	O	N/A	Channel2 AC DC coupling select external port. This port is enabled by setting the ExtRelayConfigEn parameter to "true". <ul style="list-style-type: none"> <li>• 1 = AC coupling.</li> <li>• 0 = DC coupling.</li> </ul>
sCh1GainConfig	-	O	N/A	Channel1 gain select external port. This port is enabled by setting the ExtRelayConfigEn parameter to "true". <ul style="list-style-type: none"> <li>• 1 = High Gain.</li> <li>• 0 = Low Gain.</li> </ul>
sCh2GainConfig	-	O	N/A	Channel2 gain select external port. This port is enabled by setting the ExtRelayConfigEn parameter to "true". <ul style="list-style-type: none"> <li>• 1 = High Gain.</li> <li>• 0 = Low Gain.</li> </ul>
sSync	-	I	N/A	SYNC signal control input (functionality described in Section 4.2). This port is enabled by setting the ExtSyncEn parameter to "true".
sExtSPI_Idle	-	O	N/A	Flag indicating that the configuration state machine is in the IDLE state. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sCmdDone	-	O	N/A	Pulse indicating that the SPI command has been successfully completed. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sExtSPI_TxRdEn	-	I	N/A	Read enable signal used to load data from the upper layer TX command FIFO. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sExtSPI_TxDout[23:0]	-	I	N/A	Upper layer TX command FIFO output data containing the transfer length, the register address and the register

				data that are passed to the SPI controller. This port is enabled by setting the ExtCmdInterfaceEn parameter to “true”.
sExtSPI_TxValid	-	I	N/A	Upper layer TX command FIFO data valid signal. This port is enabled by setting the ExtCmdInterfaceEn parameter to “true”.
sExtSPI_RxWrEn	-	O	N/A	Upper layer RX command FIFO write enable signal. This port is enabled by setting the ExtCmdInterfaceEn parameter to “true”.
sExtSPI_RxDin[7:0]	-	O	N/A	Upper layer RX command FIFO input data. This port is enabled by setting the ExtCmdInterfaceEn parameter to “true”.
adcClkIn_p	-	O	N/A	ADC positive differential clock input. For more details see [3]
adcClkIn_n	-	O	N/A	ADC negative differential clock input. For more details see [3]
adcSync	-	O	N/A	Synchronization signal connected to the ADC SYNC input. For more details see [3]
DcoClk	-	I	N/A	Data strobe generated by the ADC used to capture dADC_Data [3].
dADC_Data[13:0]	-	I	N/A	14bit DDR parallel data bus exported by ADC containing Channel1 and Channel 2 multiplexed samples [3].
sADC_SDIO	SPI	IO	N/A	SPI SDIO signal [3].
sADC_CS	SPI	O	N/A	SPI CS signal [3].
sADC_Sclk	SPI	O	N/A	SPI output clock [3].
sCh1CouplingH	-	O	N/A	Channel1 AC DC coupling relay driver control input.
sCh1CouplingL	-	O	N/A	Channel1 AC DC coupling select relay driver control input.
sCh2CouplingH	-	O	N/A	Channel2 AC DC coupling select relay driver control input.
sCh2CouplingL	-	O	N/A	Channel2 AC DC coupling select relay driver control input.
sCh1GainH	-	O	N/A	Channel1 gain select relay driver control input.
sCh1GainL	-	O	N/A	Channel1 gain select relay driver control input.
sCh2GainH	-	O	N/A	Channel2 gain select relay driver control input.
sCh2GainL	-	O	N/A	Channel2 gain select relay driver control input.
sRelayComH	-	O	N/A	Common relay terminal driver control input.
sRelayComL	-	O	N/A	Common relay terminal driver control input.



## 6 Parameter description

Table 3. IP core parameter descriptions.

Signal Name	Description
ExtRelayConfigEn	Enables the external relay configuration port. Set to “true” when dynamic relay configuration is required. Set to “false” when static relay configuration is sufficient.
ExtCalibEn	Enables the external calibration interface. Set to “true” when the IP core is connected to the <b>Zmod ADC 1410 AXI Adapter</b> IP core. Set to “false” when the core operates in stand alone mode.
ExtCmdInterfaceEn	Enables the upper layer IP SPI configuration interface. Set to “true” when the IP core is connected to <b>Zmod ADC 1410 AXI Adapter</b> . This will enable the processor to access the Zmod ADC 1410 SPI interface. Set to “false” when initial configuration described in Section 4.5 is sufficient.
kCh1CouplinStatic	Channel1 AC DC coupling select static configuration parameter. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. The state of the relay can not be changed afterwards. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored. <ul style="list-style-type: none"> <li>• 1 = AC coupling.</li> <li>• 0 = DC coupling.</li> </ul>
kCh2CouplinStatic	Channel2 AC DC coupling select static configuration parameter. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. The state of the relay cannot be changed afterwards. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored. <ul style="list-style-type: none"> <li>• 1 = AC coupling.</li> <li>• 0 = DC coupling.</li> </ul>
kCh1GainStatic	Channel1 gain select static configuration parameter. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. The state of the relay cannot be changed afterwards. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored. <ul style="list-style-type: none"> <li>• 1 = High Gain.</li> <li>• 0 = Low Gain.</li> </ul>
kCh2GainStatic	Channel2 gain select static configuration parameter. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. The state of the relay cannot be changed afterwards. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored. <ul style="list-style-type: none"> <li>• 1 = High Gain.</li> <li>• 0 = Low Gain.</li> </ul>
kCh1LgMultCoefStatic[17:0]	Channel1 low gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.

kCh1LgAddCoefStatic[17:0]	Channel1 low gain additive calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.
kCh1HgMultCoefStatic[17:0]	Channel1 high gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.
kCh1HgAddCoefStatic[17:0]	Channel1 high gain additive calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.
kCh2LgMultCoefStatic[17:0]	Channel2 low gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.
kCh2LgAddCoefStatic[17:0]	Channel2 low gain additive calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.
kCh2HgMultCoefStatic[17:0]	Channel2 high gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.
kCh2HgAddCoefStatic[17:0]	Channel2 high gain additive calibration coefficient. If the ExtRelayConfigEn parameter to “false”, the configuration state machine will configure the coupling select relay according to this parameter’s value at initialization time. If the value of ExtRelayConfigEn parameter is “true”, this parameter is ignored, and the processing system is expected to update the corresponding external port.

## 7 Designing with the core

### 7.1 Customization

The IP, through its customizable parameters (ExtRelayConfigEn, ExtCalibEn, ExtCmdInterfaceEn, ExtSyncEn), enables the user to opt for a more basic design with minimal external ports or a more configurable but also more complex design with several ports that enable dynamic configuration of several hardware features. When using the IP Core with the Zmod ADC 1410 AXI adapter, the hardware configuration features are expected to be controlled by the processing system, so all interfaces should be enabled and connected to the upper layer IP Core.

## 8 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.4, May 13, 2014.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Analog Devices, AD9648 Datasheet, Rev C.
4. Xilinx Inc., UG903: Using Constraints, v2014.3, October 31, 2014