

IP-Konfiguration Milestone 6

axis_slave_simmodel_v1_0 (1.0)

Documentation IP Location

Show disabled ports

Component Name: SIM_Environment/axis_slave_simmodel_0

Page: Framing - **AXIS and FIFO**

File Name: J.J.J.Jst_out

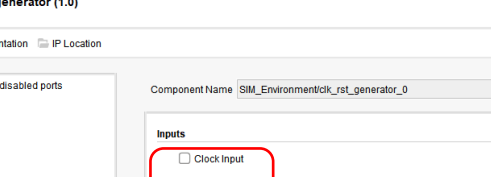
☐ File Autoincrementing

File Extension

☒ bmp
☐ yuv
☐ bin
☐ raw

Num Pix Per Line: 192
 Num Lines: 192
 Pixel Format: 13
 Num Files: 1
 Num Frames Per File: 1

OK Cancel



The screenshot shows the 'Re-customize IP' dialog for the 'clk_rst_generator' component. The component name is 'SIM_Environment/clk_rst_generator_0'. Under the 'Inputs' section, the 'Stop Input' checkbox is checked and highlighted with a red rectangle. The 'Generated Clock Period' is set to 10000 ps. The 'stop_simulation' block is connected to the 'rst_n' input.

Re-customize IP

axil_master_with_rom (1.0)

Documentation IP Location

☐ Show disabled ports

Component Name

Stimuli Filename

Stim Filename

The given filename will be used for synthesis as is and prefixed by "../.." for simulation

IO

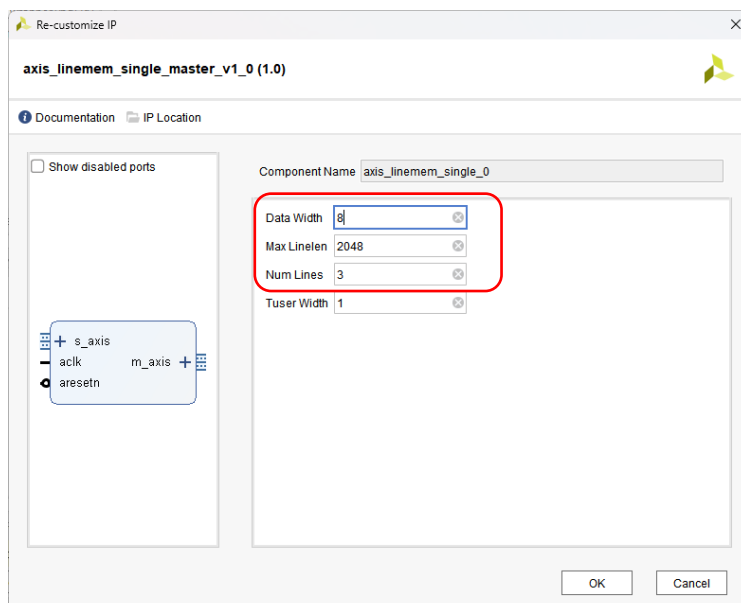
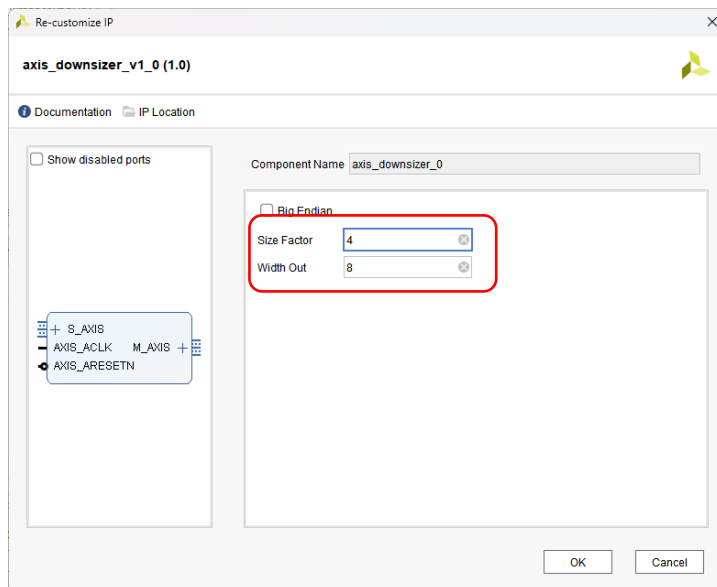
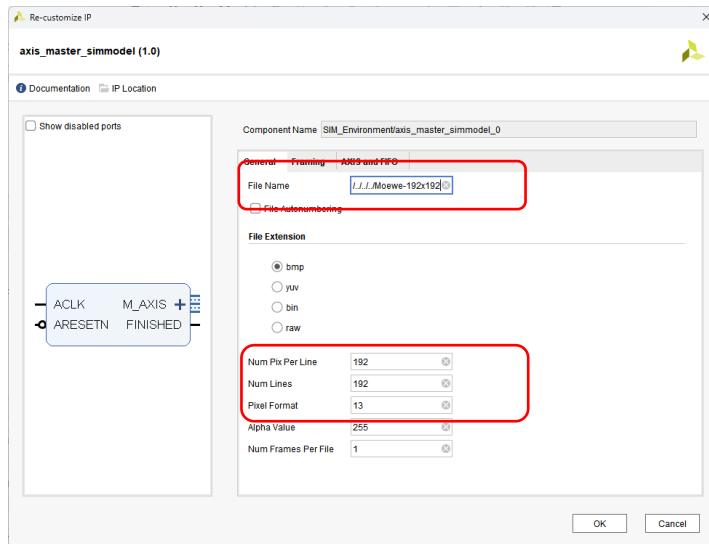
☐ Has Finished Out

☐ Has Interrupt In

☐ M_AXIL_ACLK M_AXIL_ARESETN M_AXIL

OK Cancel

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